Product Specifications

17.0" SXGA Color TFT-LCD Smart Integration Module
Model Name: M170ES04
V.1

( ) Preliminary Specifications
(◆) Final Specifications

i Contents

ii Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1. 2001/10/04	All	First Edition for Customer	All	
0.2. 2002/01/21	5,8	Interface connector: JAE or compatible	Interface connector: **Hirose or compatible**	Change
0.3 2002/01/21	22	n.a	Product label	Add
0.4 2002/01/30	4	n.a.	Weight: 2000g	Add

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT-LCD module.

10) After installation of the TFT-LCD module into an enclosure (LCD monitor housing, for example), do not twist nor bend the TFT -LCD module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT -LCD module from outside. Otherwise the TFT -LCD module may be damaged.

2.0 General Description

This specification applies to the 17.0 inch Color TFT-LCD Integration Module M170ES04.
The display supports the SXGA (1280(H) x 1024(V)) screen format and 16.7M colors (RGB 8-bits data).
All input signals are TTL interface compatible.
This module does not contain an inverter card for backlight.

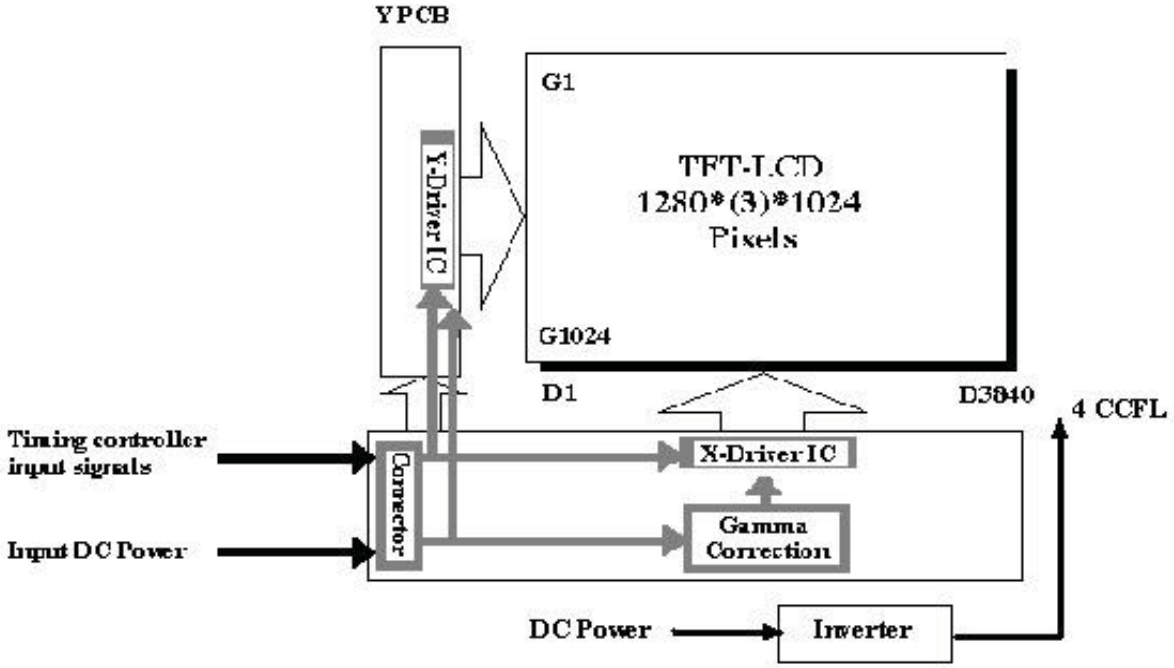
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	432(17.0")
Active Area	[mm]	337.920 (H) x 270.336(V)
Pixels H x V		1280(x3) x 1024
Pixel Pitch	[mm]	0.264 (per one triad) x 0.264
Pixel Arrangement Display Mode		R.G.B. Vertical Stripe Normally White
White Luminance Contrast Ratio	[cd/m^2]	250 (Typ) 400 : 1 (Typ)
Optical Response Time	[msec]	40 (Typ)
Physical Size	[mm]	383.5(W) x 306(H) x 20.0(D) (Typ)
Weight	[g]	2000 (Typ)
Electrical Interface		Even-Even R/G/B data (8bits) Even-Odd R/G/B data (8bits) Odd-Even R/G/B data (8bits) Odd-Odd R/G/B data (8bits), 15 timing control signal input 4 DC power input
Support Color		16.7M colors (RGB 8-bit data)
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches Color TFT-LCD Smart Module:



X PCB
Hirose FH12-30S
Hirose FH12-50S

JST BHR-04VS-1
Mating Type SM04 (4.0) B-BHS-1-TB

2.3 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	60/60 -	70/70	- -
	[degree] [degree]	Vertical (Up) CR = 10 (Down)	50 55	60 65	- -
	[degree] [degree]	Horizontal (Right) CR = 5 (Left)	70 -	80	- -
	[degree] [degree]	Vertical (Up) CR = 5 (Down)	70 -	80	- -
Contrast ratio		Normal Direction	250	400	-
Response Time	[msec] [msec] [msec]	Raising Time Falling Time Raising + Falling	- - -	25 15 40	35- 25- -
Color / Chromaticity Coordinates (CIE)		Red x	0.59	0.62	0.65
		Red y	0.3	0.33	0.36
		Green x	0.27	0.30	0.33
		Green y	0.57	0.60	0.63
		Blue x	0.12	0.15	0.18

		Blue y	0.07	0.10	0.13
Color Coordinates (CIE) White		White x	0.28	0.31	0.34
		White y	0.3	0.33	0.36
Luminance Uniformity (Note 1)	[%]		80	85	-
White Luminance at CCFL 6.0mA(center point)	[cd/m^2]		200	250	-
Crosstalk (in 75Hz)	[%]				1.5

Note 1 Measure points & Diagram

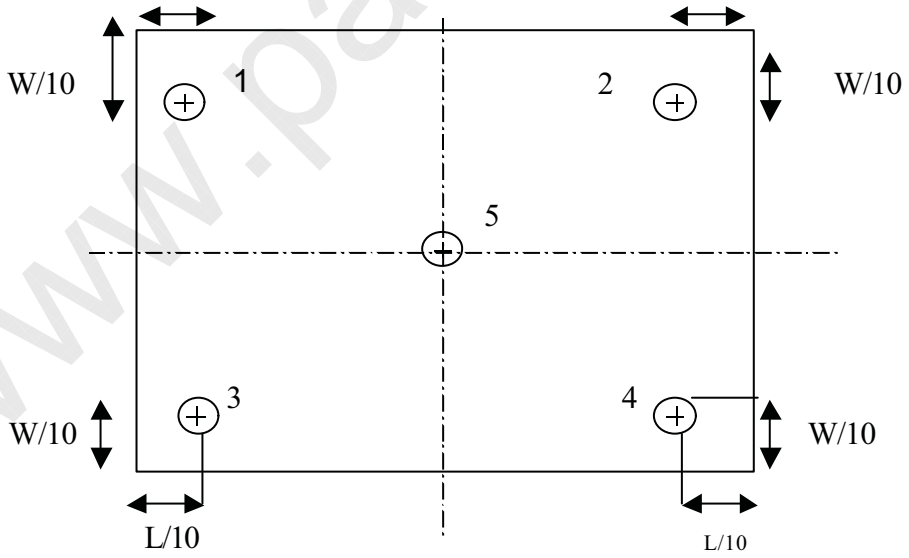
$$x = \frac{\text{Display Length distance}}{10}$$

$$y = \frac{\text{Display Width distance}}{10}$$

$$\text{Uniformity} = \frac{\text{Minimum Luminance in 5 Points (1-5)}}{\text{Maximum Luminance in 5 Points (1-5)}}$$

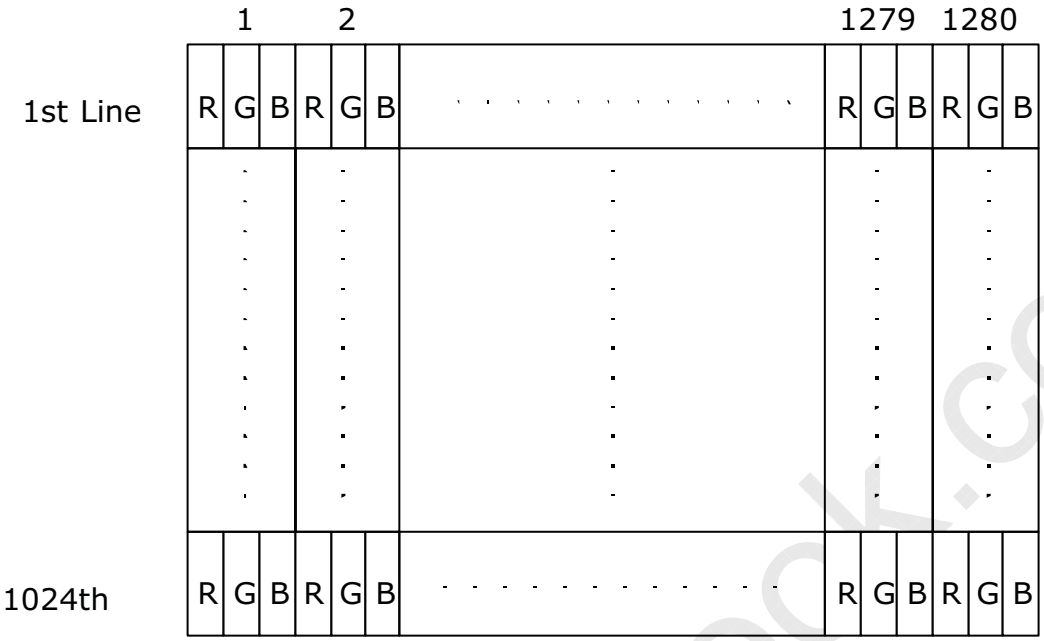
This panel is compatible with TCO99 approbation in luminance uniformity <1.7, luminance contrast >0.5

LCD Display area = 337.9 x 270.4 mm



2.4 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format.



3.0 Electrical characteristics

3.1 Absolute Maximum Ratings (GND=0V)

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage (1)	V33	-0.3	4.6	[Volt]	
Supply Voltage (2)	AVDD	-0.3	15	[Volt]	
Supply Voltage (3)	YV1	-0.3	42	[Volt]	
Supply Voltage (4)	YVEE	-16	0.3	[Volt]	
	YV1-YVEE	-0.3	42	[Volt]	
CCFL Inrush current	ICFLL	-	38	[mA]	Note 1
CCFL Current	ICFL	-	7.6	[mA] rms	
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	8	95	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	8	95	[%RH]	Note 2

Note 1 : Duration=50 msec.
Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.
Note3 : Source-Driver IC : T6L64 , Gate-Driver IC : TMS57606

3.2 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be will be following components.

J5

Connector Name / Designation	**Interface Connector / X-PCB card**
Manufacture	**Hirose or compatible**
Type Part Number	**FH12-30S**

J6,J7

Connector Name / Designation	**Interface Connector / X-PCB card**
Manufacture	**Hirose or compatible**
Type Part Number	**FH12-50S**

3.3 Signal Pin

J5 CONNECTOR

Pin#	Signal Name	Pin#	Signal Name
1	XOEG6	2	XOEG5
3	XOEG4	4	XOEG3
5	XOEG2	6	XOEG1
7	XOEG0	8	GND
9	XOEB7	10	XOEB6
11	XOEB5	12	XOEB4
13	XOEB3	14	XOEB2
15	XOEB1	16	XOEB0

17	V33	18	V33
19	V33	20	AVDD
21	AVDD	22	AVDD
23	YV1	24	YVEE
25	GND	26	GATE-ON
27	YOE	28	YCLK
29	YDIO2	30	YDIO1

J6 CONNECTOR

Pin#	Signal Name	Pin#	Signal Name
1	EPOL	2	ELOAD
3	EDO/I	4	GND
5	XECLK	6	GND
7	XEDINV	8	GND
9	XOOR7	10	XOOR6
11	XOOR5	12	XOOR4
13	XOOR3	14	XOOR2
15	XOOR1	16	XOOR0
17	XOOG7	18	XOOG6
19	XOOG5	20	XOOG4
21	XOOG3	22	XOOG2
23	XOOG1	24	XOOG0
25	GND	26	XOOB7
27	XOOB6	28	XOOB5
29	XOOB4	30	XOOB3
31	XOOB2	32	XOOB1
33	XOOB0	34	OPOL
35	OLOAD	36	ODO/I
37	GND	38	XOCLK
39	GND	40	XODINV
41	GND	42	XOER7
43	XOER6	44	XOER5
45	XOER4	46	XOER3
47	XOER2	48	XOER1
49	XOER0	50	XOEG7

J7 CONNECTOR

Pin#	Signal Name	Pin#	Signal Name
1	XEOR7	2	XEOR6
3	XEOR5	4	XEOR4
5	XEOR3	6	XEOR2
7	XEOR1	8	XEOR0
9	XEOG7	10	XEOG6
11	XEOG5	12	XEOG4
13	XEOG3	14	XEOG2
15	XEOG1	16	XEOG0
17	GND	18	XEOB7
19	XEOB6	20	XEOB5
21	XEOB4	22	XEOB3
23	XEOB2	24	XEOB1
25	XEOB0	26	XEER7

27	XEER6	28	XEER5
29	XEER4	30	XEER3
31	XEER2	32	XEER1
33	XEER0	34	GND
35	XEEG7	36	XEEG6
37	XEEG5	38	XEEG4
39	XEEG3	40	XEEG2
41	XEEG1	42	XEEG0
43	XEEB7	44	XEEB6
45	XEEB5	46	XEEB4
47	XEEB3	48	XEEB2
49	XEEB1	50	XEEB0

3.4 Signal Description

J7 CONNECTOR

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	XEOR7	Red Data bit 7 (Even-Odd)	2	XEOR6	Red Data bit 6 (Even-Odd)
3	XEOR5	Red Data bit 5 (Even-Odd)	4	XEOR4	Red Data bit 4 (Even-Odd)
5	XEOR3	Red Data bit 3 (Even-Odd)	6	XEOR2	Red Data bit 2 (Even-Odd)
7	XEOR1	Red Data bit 1 (Even-Odd)	8	XEOR0	Red Data bit 0 (Even-Odd)
9	XEOG7	Green Data bit 7 (Even-Odd)	10	XEOG6	Green Data bit 6 (Even-Odd)
11	XEOG5	Green Data bit 5 (Even-Odd)	12	XEOG4	Green Data bit 4 (Even-Odd)
13	XEOG3	Green Data bit 3 (Even-Odd)	14	XEOG2	Green Data bit 2 (Even-Odd)
15	XEOG1	Green Data bit 1 (Even-Odd)	16	XEOG0	Green Data bit 0 (Even-Odd)
17	GND	Ground	18	XEOB7	Blue Data bit 7 (Even-Odd)
19	XEOB6	Blue Data bit 6 (Even-Odd)	20	XEOB5	Blue Data bit 5 (Even-Odd)
21	XEOB4	Blue Data bit 4 (Even-Odd)	22	XEOB3	Blue Data bit 3 (Even-Odd)
23	XEOB2	Blue Data bit 2 (Even-Odd)	24	XEOB1	Blue Data bit 1 (Even-Odd)
25	XEOB0	Blue Data bit 0 (Even-Odd)	26	XEER7	Red Data bit 7 (Even-Even)
27	XEER6	Red Data bit 6 (Even-Even)	28	XEER5	Red Data bit 5 (Even-Even)
29	XEER4	Red Data bit 4 (Even-Even)	30	XEER3	Red Data bit 3 (Even-Even)
31	XEER2	Red Data bit 2 (Even-Even)	32	XEER1	Red Data bit 1 (Even-Even)
33	XEER0	Red Data bit 0 (Even-Even)	34	GND	Ground
35	XEEG7	Green Data bit 7 (Even-Even)	36	XEEG6	Green Data bit 6 (Even-Even)
37	XEEG5	Green Data bit 5 (Even-Even)	38	XEEG4	Green Data bit 4 (Even-Even)
39	XEEG3	Green Data bit 3 (Even-Even)	40	XEEG2	Green Data bit 2 (Even-Even)
41	XEEG1	Green Data bit 1 (Even-Even)	42	XEEG0	Green Data bit 0 (Even-Even)
43	XEEB7	Blue Data bit 7 (Even-Even)	44	XEEB6	Blue Data bit 6 (Even-Even)
45	XEEB5	Blue Data bit 5 (Even-Even)	46	XEEB4	Blue Data bit 4 (Even-Even)
47	XEEB3	Blue Data bit 3 (Even-Even)	48	XEEB2	Blue Data bit 2 (Even-Even)
49	XEEB1	Blue Data bit 1 (Even-Even)	50	XEEB0	Blue Data bit 0 (Even-Even)

J6 CONNECTOR

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	EPOL	Source driver output polarity control (Even)	2	ELOAD	Source driver latch pulse (Even)

3	EDO/I	Horizontal Start Pulse (Even)	4	GND	Ground
5	XECLK	Pixel Clock Input (Even)	6	GND	Ground
7	XEDINV	Data Reverse Control Signal (Even)	8	GND	Ground
9	XOOR7	Red Data bit 7 (Odd-Odd)	10	XOOR6	Red Data bit 6 (Odd-Odd)
11	XOOR5	Red Data bit 5 (Odd-Odd)	12	XOOR4	Red Data bit 4 (Odd-Odd)
13	XOOR3	Red Data bit 3 (Odd-Odd)	14	XOOR2	Red Data bit 2 (Odd-Odd)
15	XOOR1	Red Data bit 1 (Odd-Odd)	16	XOOR0	Red Data bit 0 (Odd-Odd)
17	XOOG7	Green Data bit 7 (Odd-Odd)	18	XOOG6	Green Data bit 6 (Odd-Odd)
19	XOOG5	Green Data bit 5 (Odd-Odd)	20	XOOG4	Green Data bit 4 (Odd-Odd)
21	XOOG3	Green Data bit 3 (Odd-Odd)	22	XOOG2	Green Data bit 2 (Odd-Odd)
23	XOOG1	Green Data bit 1 (Odd-Odd)	24	XOOG0	Green Data bit 0 (Odd-Odd)
25	GND	Ground	26	XOOB7	Blue Data bit 7 (Odd-Odd)
27	XOOB6	Blue Data bit 6 (Odd-Odd)	28	XOOB5	Blue Data bit 5 (Odd-Odd)
29	XOOB4	Blue Data bit 4 (Odd-Odd)	30	XOOB3	Blue Data bit 3 (Odd-Odd)
31	XOOB2	Blue Data bit 2 (Odd-Odd)	32	XOOB1	Blue Data bit 1 (Odd-Odd)
33	XOOB0	Blue Data bit 0 (Odd-Odd)	34	OPOL	Source driver output polarity control (Odd)
35	OLOAD	Source driver latch pulse (Odd)	36	ODO/I	Horizontal Start Pulse (Odd)
37	GND	Ground	38	XOCLK	Pixel Clock Input (Odd)
39	GND	Ground	40	XODINV	Data Reverse Control Signal (Odd)
41	GND	Ground	42	XOER7	Red Data bit 7 (Odd-Even)
43	XOER6	Red Data bit 6 (Odd-Even)	44	XOER5	Red Data bit 5 (Odd-Even)
45	XOER4	Red Data bit 4 (Odd-Even)	46	XOER3	Red Data bit 3 (Odd-Even)
47	XOER2	Red Data bit 2 (Odd-Even)	48	XOER1	Red Data bit 1 (Odd-Even)
49	XOER0	Red Data bit 0 (Odd-Even)	50	XOEG7	Green Data bit 7(Odd-Even)

J5 CONNECTOR

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	XOEG6	Green Data bit 6 (Odd-Even)	2	XOEG5	Green Data bit 5 (Odd-Even)
3	XOEG4	Green Data bit 4 (Odd-Even)	4	XOEG3	Green Data bit 3 (Odd-Even)
5	XOEG2	Green Data bit 2 (Odd-Even)	6	XOEG1	Green Data bit 1 (Odd-Even)
7	XOEG0	Green Data bit 0 (Odd-Even)	8	GND	Ground
9	XOEB7	Blue Data bit 7 (Odd-Even)	10	XOEB6	Blue Data bit 6 (Odd-Even)
11	XOEB5	Blue Data bit 5 (Odd-Even)	12	XOEB4	Blue Data bit 4 (Odd-Even)
13	XOEB3	Blue Data bit 3 (Odd-Even)	14	XOEB2	Blue Data bit 2 (Odd-Even)
15	XOEB1	Blue Data bit 1 (Odd-Even)	16	XOEB0	Blue Data bit 0 (Odd-Even)
17	V33	Digital Power Input (DC +3.3V)	18	V33	Digital Power Input (DC +3.3V)
19	V33	Digital Power Input (DC +3.3V)	20	AVDD	Analog Power Input (DC +12.5V)
21	AVDD	Analog Power Input (DC +12.5V)	22	AVDD	Analog Power Input (DC +12.5V)
23	YV1	Gate Driver High Voltage Input (DC +26.5V)	24	YVEE	Gate Driver Low Voltage Input (DC -6V)
25	GND	Ground	26	GATE-ON	Gate Driver Output Enable Signal
27	YOE	Gate Driver output	28	YCLK	Gate Driver Pixel Clock Input

		Enable Signal			
29	YDIO2	Vertical Start Pulse 2	30	YDIO1	Vertical Start Pulse 1
25	GND	Ground	26	GATE-ON	Gate Driver Output Enable Signal

3.5 Signal Electrical Characteristic

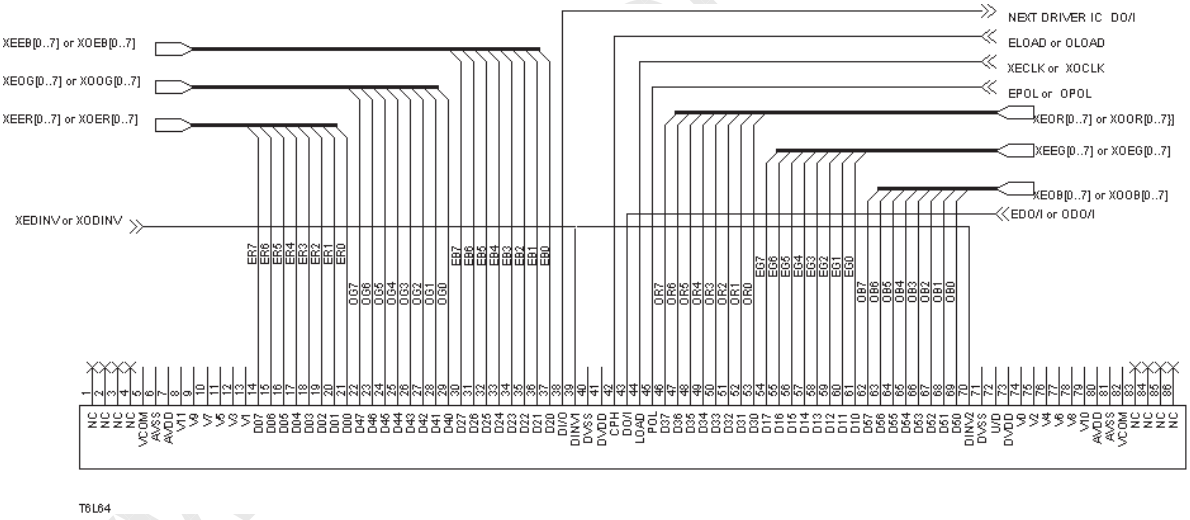
It is recommended to refer the specifications of source driver(Toshiba:T6L64) and gate driver(TI:TMS57606) in detail.

Characteristics		SYMBOL	MIN	TYP.	MAX	UNIT
Input Voltage	Low Level	VIL	0		0.3XV33	Volt
	High Level	VIH	0.7XV33		V33	Volt

3.6 Interface Timing

3.6-1 Timing Characteristics

Make sure the setup and hold time of each source driver input signal fit the following specification. The electrical diagram below is TAB pin assignment.



3.6-2 Source and Gate Driver Timing Requirement

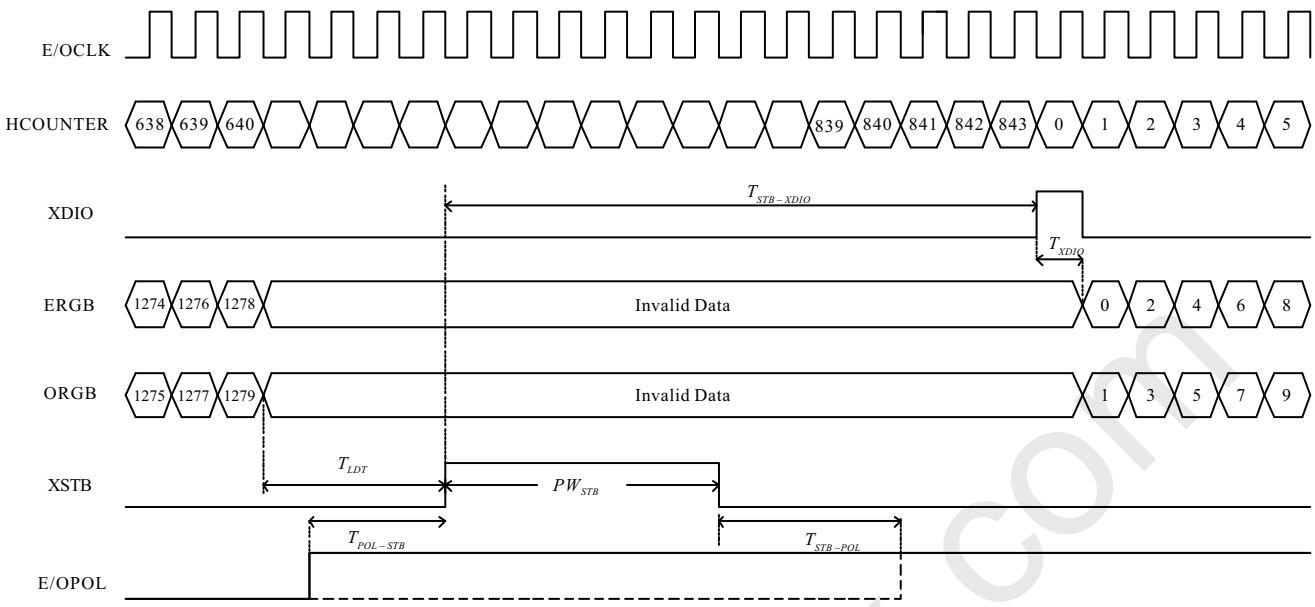
This following data describes the source and gate drivers timing requirement for 17" XGA (1280 × 1024) Panel. The control timing is defined based on VESA SXGA at frame rate 75 Hz(non-interlaced). The symbols and timing requirement are defined in Table 1 and Table 2. And, the timing diagrams for the source and gate drivers are shown in Figure 1 and Figure 2 respectively.

Table 1. Timing requirement for Source Driver

Parameter	Symbol	Condition	Min.	TYP.	MAX.	Unit
Clock Width(H)	T_{CWH}	V_{IH} to V_{IH}	4			ns
Clock Width(L)	T_{CWL}	V_{IL} to V_{IL}	4			ns
Clock and Data Setup Time	T_{Setup}		4			ns
Clock and Data Hold Time	T_{Hold}		0			ns
XDIO Position	T_{XDIO}	XDIO ↑ → First Data	1	1	1	CLK
XSTB Pulse Width	PW_{STB}			1.0		μs
			2			CLK
Last Data Timing	T_{LDT}	Last Data → XSTB ↑	2			CLK
POL-XSTB Time	$T_{POL-STB}$	POL ↑ or ↓ →XSTB ↑	4			ns
XSTB-XPOL Time	$T_{STB-POL}$	XSTB ↓ →POL ↑ or ↓	0			ns
XSTB- XDIO Time	$T_{STB-XDIO}$	XSTB ↑ → XDIO ↑	2			CLK

Table 2. Timing requirement for Gate Driver

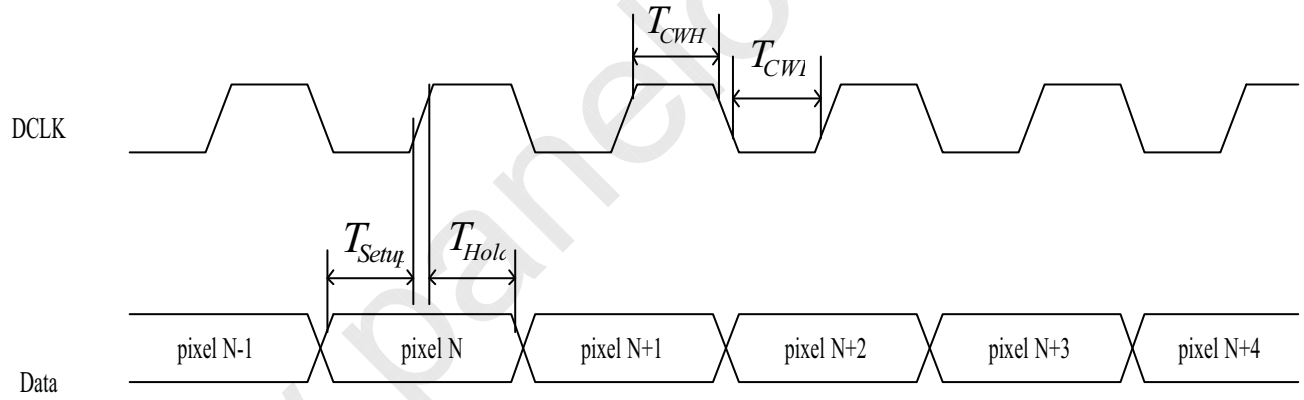
Parameter	Symbol	Condition	Min.	TYP.	MAX.	Unit
Clock Pulse Width (High)	T_{CLKH}		1	2.6		μs
Clock Pulse Width (Low)	T_{CLKL}		4			μs
YOE Pulse Width (Low)	T_{YOEL}			2.6		μs
YCLK rising to XSTB rising	T_1			1.7		μs
YCLK falling to XSTB falling	T_2			100		ns
YCLK rising to YOE falling	T_3			240		ns
YCLK falling to YOE rising	T_4			240		ns
Gate On to Source Out	$T_{YOE-STB}$	YOE ↑ →XSTB ↓		-1.2		us
YDIO start time	$T_{YDIO-DE}$	YDIO ↑ →first line(DE)		3		Line



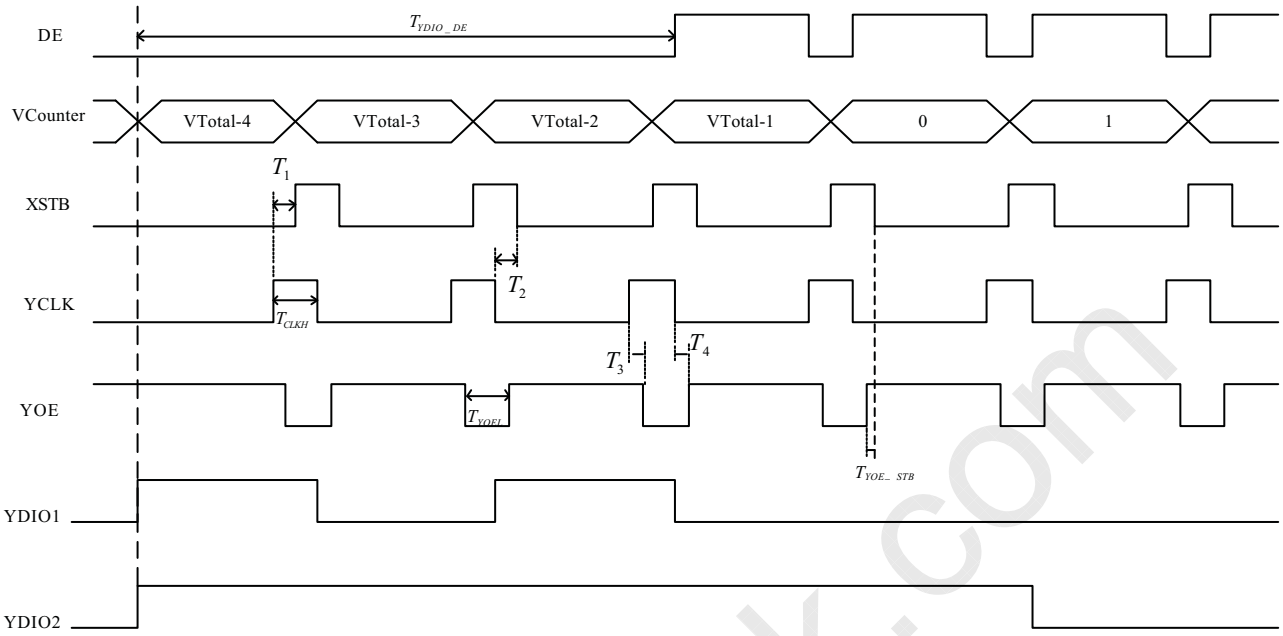
Note1 : HCOUNTER is reference signal

Note2 : For SXGA@75Hz Htotal = 1688 pixels

Source Driver Timing
Figure 1



Source Driver Timing
Figure1(cont.)



Note1 : DE and VCounter are reference signals

Note2 : For SXGA@75Hz Vtotal= 1066 lines

Gate Driver Timing
Figure 2

3.7 Power Consumption

Recommend Operating Condition (GND=0V)

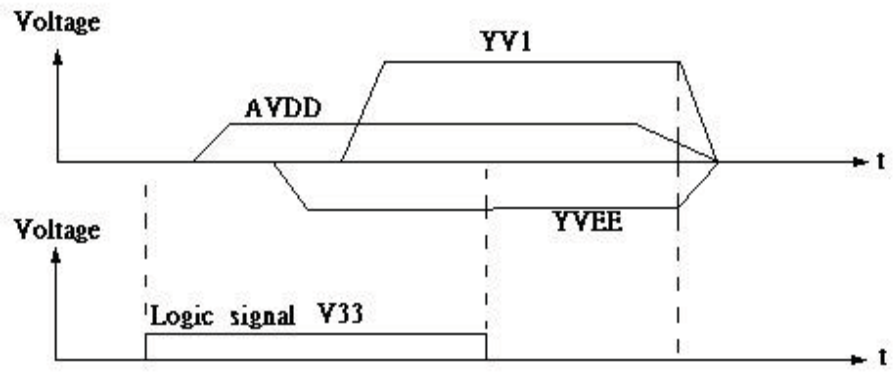
Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage (1)	V33	3	3.3	3.6	[Volt]	*Ripple<80mV
Supply Voltage (2)	AVDD	9.1	9.6	10.1	[Volt]	*Ripple<200mV
Supply Voltage (3)	YV1	23.8	25.09	26.3	[Volt]	*Ripple<80mV
Supply Voltage (4)	YVEE	-4.7	-4.95	-5.2	[Volt]	*Ripple<80mV
V33 Current	I_{V33}	-	35	70	[mA] rms	V33=3.3V
AVDD Current	I_{AVDD}	-	320	640	[mA] rms	AVDD=9.6V
YV1 Current	I_{YV1}	-	5	10	[mA] rms	YV1=25.09V
YVEE Current	I_{YVEE}	-	-5	10	[mA] rms	YVEE=-4.95V

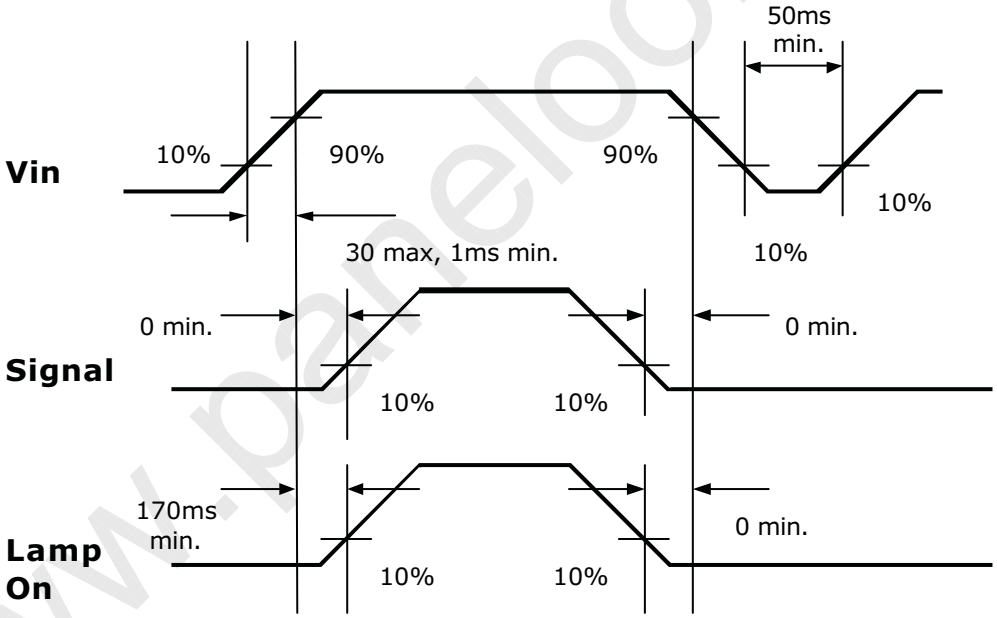
***Ripple amplitude is tested under the worst case.**

3.8 Power ON/OFF Sequence

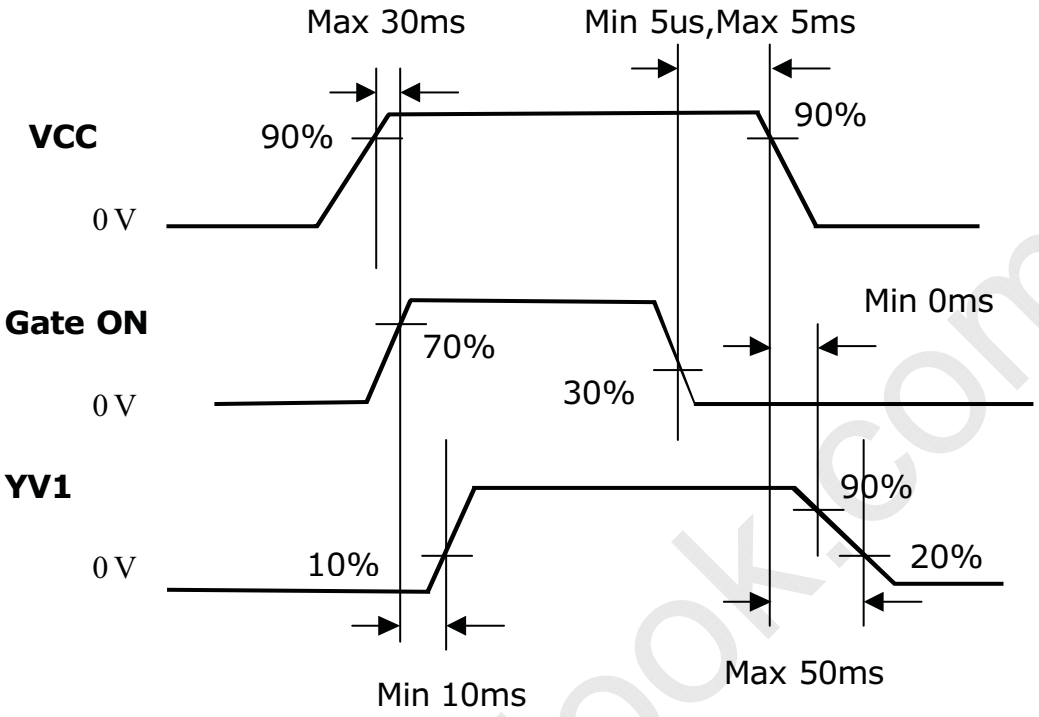
Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart.

When the device is power on, the sequence should be: logic signal(V33)→ AVDD→ YVEE→ YV1





3.9 Gate ON & YV1 Timing



4.0 Backlight Characteristics

4.1 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp High Voltage
3	No Connection
4	Ground

4.2 Parameter guide line for CFL Inverter

Symbol	Parameter	Min	Typ	Max	Units	Condition
(L255)	White Luminance	200	250	-	[cd/m²]	(Ta=25°C)
ISCFL	CCFL standard current	5.5	6.0	6.5	[mA] rms	(Ta=25°C)
IRCFL	CCFL operation range	3.0	6.0	7.0	[mA] rms	(Ta=25°C)
ICFL	CCFL Inrush current	-	26	34	[mA]	Note 1
fCFL	CCFL Frequency	40	50	80	[KHz]	(Ta=25°C) Note 2
ViCFL (0°C)	CCFL Ignition Voltage	1700			[Volt] rms	(Ta=0°C) Note 4
ViCFL (25°C)	CCFL Ignition Voltage	1200			[Volt] rms	(Ta=25°C) Note 4
VCFL	CCFL Discharge Voltage (Reference)		720	863	[Volt] rms	(Ta=25°C) Note 3
PCFL	CCFL Power consumption		17.3	19.0	[Watt]	(Ta=25°C) Note 3

Note 1: Duration=50 [msec]
Note 2: CCFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD
Note 3: Calculator value for reference (ICFL×VCFL=PCFL)
Note 4: CCFL inverter should be able to give out a power that has a generating capacity of over 1700 voltage. Lamp units need 1700 voltage minimum for ignition

5.0 Vibration, Shock, and Drop

5.1 Vibration & Shock

Frequency: 10 - 200Hz
Sweep: 30 Minutes each Axis (X, Y, Z)
Acceleration: 1.5G(10~200Hz P- P)
Test method:

Acceleration (G)	1.5
Frequency (Hz)	10~200~10
Active time(min)	30

5.2 Shock Test Spec:

Acceleration (G) –a	50
Active time -b	20
Wave form	half-sin
Times	1

Direction: ±X, ±Y, ±Z

5.3 Drop test

Package test: The drop height is 60 cm.

6.0 Environment

The display module will meet the provision of this specification during operating condition or after storage or shipment condition specified below. Operation at 10% beyond the specified range will not cause physical damage to the unit.

6.1 Temperature and Humidity

6.1.1 Operating Conditions

The display module operates error free, when operated under the following conditions;

Temperature 0 ^{0}C to 50 ^{0}C
Relative Humidity 8% to 95%
Wet Bulb Temperature 39.0 ^{0}C

6.1.2 Shipping Conditions

The display module operates error free, after the following conditions;

Temperature -20 ^{0}C to 60 ^{0}C
Relative Humidity 8% to 95%
Wet Bulb Temperature 39.0 ^{0}C

6.2 Atmospheric Pressure

The display assembly is capable of being operated without affecting its operations over the pressure range as following specified;

	Pressure	Note
Maximum Pressure	1040hPa	0m = sea level
Minimum Pressure	674hPa	3048m = 10.000 feet

Note : Non-operation attitude limit of this display module = 30,000 feet. = 9145 m.

6.3 Thermal Shock

The display module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20^{0}C to 60^{0}C, and back again.

Thermal shock cycle -20 ^{0}C for 30min
60 ^{0}C for 30min

Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before powering on.

7.0 Reliability

This display module and the packaging of that will comply following standards.

7.1 Failure Criteria

The display assembly will be considered as failing unit when it no longer meets any of the requirements stated in this specification. Only as for maximum white luminance, following criteria is applicable.

Note : Maximum white Luminance shall be 125 cd/m^{2}or more.

7.2 Failure Rate

The average failure rate of the display module (from first power-on cycle till 1,000 hours later) will not exceed 1.0%.
The average failure rate of the display module from 1,000 hours until 16,000 hours will not exceed 0.7%
per 1000 hours.

7.2.1 Usage

The assumed usage for the above criteria is:

220 power-on hours per month
500 power on/off cycles per month
Maximum brightness setting
Operation to be within office environment (25^{0}C typical)

7.2.2 Component De-rating

All the components used in this device will be checked the load condition to meet the failure rate criteria.

7.3 CCFL Life

The assumed CCFL Life will be longer than 30,000 hours, typical value is 50,000 hours under stable condition at 25 ± 5^{o}C;
Standard current at 6.0 ± 0.5mA.
Definition of life: brightness becomes 50% or less than the minimum luminance value of CCFL.

7.4 ON/OFF Cycle

The display module will be capable of being operated over the following ON/OFF Cycles.

ON/OFF	Value	Cycles
+Vin and CCFL power	30,000	10 seconds on / 10 seconds off

8.0 Safety

8.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

8.2 Materials

8.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible ADT Toxicologist.

8.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process. The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

8.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

8.4 Hazardous Voltages

Any point exceeding 42.4 volts meets the requirement of the limited current circuit. The current through a 2KΩ resistance is less than 0.7 x f (kHz) mA.

9.0 Other requirements

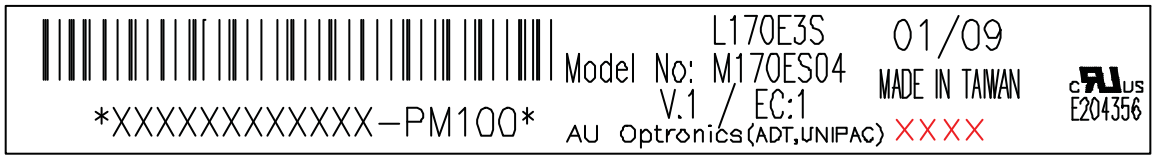
9.1 National Test Lab Requirement

The display module will satisfy all requirements for compliance to

UL 1950, First Edition	U.S.A. Information Technology Equipment
CSA C22.2 No. 950-M89	Canada, Information Technology Equipment
EEC 950	International, Information Technology Equipment
EN 60 950	International, Information Processing Equipment (European Norm for IEC950)

9.2 Label

9.2.1 Product label



10.0 Mechanical Characteristics